**Problem 1.** We examine how pipelining affects the clock cycle time of the processor. Let us assume that individual stages of the datapath have the following latencies:

IF: 250ps  
ID: 350ps  
EX: 150ps  
MEM: 300ps  
WB: 200ps

1. What is the clock cycle time in a pipelined and non-pipelined processor?

Pipelined:

350ps

Non-Pipelined:

1250ps

1. What is the total latency of an LW instruction in a pipelined and non-pipelined processor?

Pipelined:

350\*5 = 1750ps

Non-Pipelined:

250+350+150+300+200 = 1250ps

1. If we can split one stage of the pipelined datapath into two new stages, each with half the latency of the original stage, which stage would you split and what is the new clock cycle time of the processor?

The stage that you should split is the ID stage since it has the highest latency. The new clock cycle of the processor will be 300ps since MEM would have the highest latency after the split.